LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A method for fabricating a precision polysilicon resistor comprising:

providing a structure that includes at least one polysilicon resistor device region and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer;

selectively performing an ion implant and an activation anneal in the at least one other type of device region forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor;

forming a protective dielectric layer overlying said polysilicon layer in said at least one polysilicon resistor device region; and

providing a predetermined resistance value to said polysilicon layer in said at least one polysilicon resistor device region.

Claim 2 (Original) The method of Claim 1 wherein said at least one polysilicon device region comprises a semiconductor substrate, an optional first dielectric located on the substrate, said polysilicon layer located on the substrate or the optional first dielectric and a second dielectric layer located on the polysilicon layer.

Claim 3 (Cancelled)

Claim 4 (Original) The method of Claim 1 further comprising forming a patterned photoresist atop the at least one polysilicon resistor device region to protect the region during said selective ion implant.

Claim 5 (Original) The method of Claim 1 wherein said protective dielectric layer is a nitride.

Claim 6 (Original) The method of Claim 1 wherein said step of providing a predetermined resistance value to said polysilicon layer comprises ion implantation into the polysilicon layer.

Claim 7 (Original) The method of Claim 6 wherein said ion implantation comprises p or n-type dopants.

Claim 8 (Original) The method of Claim 7 wherein said ion implantation provides said polysilicon layer with a dopant concentration of from about $1x10^{14}$ to about $1x10^{21}$ atom/cm^3.

Claim 9 (Original) The method of Claim 6 further comprising an annealing step after said ion implantation.

Claim 10 (Original) The method of Claim 9 wherein said annealing step is performed in an inert gas ambient that may optionally be mixed with less than about 10% oxygen.

Claim 11 (Original) The method of Claim 1 further comprising exposing end portions of said polysilicon layer after said step of providing a predetermined resistance value to said polysilicon layer.

Claim 12 (Original) The method of Claim 11 further comprising providing silicide contacts on the exposed polysilicon layer.

Claim 13 (Original) The method of Claim 12 wherein said silicide contacts are formed using a silicidation process.

Claim 14 (Original) The method of Claim 13 wherein said silicidation process comprises depositing a conductive metal and annealing to cause reaction of the conductive metal with the underlying polysilicon layer thereby forming said silicide contacts.

Claim 15 (Original) The method of Claim 14 wherein said conductive metal is selected from the group consisting of Co, Ni, Ti, W and alloys thereof.

Claim 16 (Original) The method of Claim 15 wherein said conductive metal is Co or Ti.

Claim 17 (Currently Amended) A process for fabricating a precision polysilicon resistor comprising:

performing a rapid thermal anneal for an emitter/FET activation process on a wafer or chip having a partially formed polysilicon resistor having a polysilicon layer, said rapid thermal anneal forming at least one of an emitter of a bipolar transistor, a polysilicon gate of a field effect transistor or source/drain regions of said field effect transistor;

depositing a protective layer over the polysilicon layer to protect the polysilicon layer against subsequent silicide processing;

ion implanting a dopant into the polysilicon layer through the protective layer; and

performing silicide processing to form the precision polysilicon resistor.

Claim 18 (Original) The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal to activate the resistor polysilicon ion implant dopant.

Claim 19 (Original) The method of Claim 17 wherein the step of performing silicide processing includes performing a silicide formation thermal anneal followed by a silicide conversion thermal anneal.

Claim 20 (Original) The method of Claim 17 wherein said protective layer comprises a nitride.